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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,010	12/13/2001	Scott Derner	400.119US01	2780

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,010	DERNER ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *1-8 and 15-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-14 and 24-26* is/are rejected.

7)☒ Claim(s) *11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-5, drawn to ROM Embedded DRAM wherein ROM Cells are Formed by Programming DRAM Cells within a DRAM Array and Correction Circuitry is Fabricated on and Integrated with the DRAM, classified in class 365, subclass 201.

   II. Claims 6-8, drawn to Method of Fabricating a ROM Embedded DRAM by Forming an Array of DRAM Cells having a First Portion of ROM Cells and a Second Portion of DRAM Cells and Programming a ROM Portion of the DRAM Cells as ROM Bits, classified in class 716, subclass 8.

   III. Claims 9-14 and 24-26, drawn to A Method of Operating a ROM Embedded DRAM by Receiving a Row and Column Address to Read Data from a ROM Section and Reading an Encoded ROM Bit, classified in class 714, subclass 773. Note: the Attorney informed the Examiner that the Applicant had intended claim 11 to depend from claim 10 (see Interview Summary).

   IV. Claims 15-17, drawn to ROM Embedded DRAM with an Error Correction Element Containing Encoded ROM Bit Data or each ROM Bit, classified in class 714, subclass 763.

V. Claims 18-21, drawn to A Method of Repairing ROM Bit Errors in a ROM Embedded DRAM by Encoding ROM Data in Error Correction Circuitry, Determining Whether the ROM Bit Data is Correct and Correcting the ROM Bit Data if the ROM Bit Data and the Stored Data Are Different, classified in class 714, subclass 763.

VI. Claims 22 and 23, drawn to A Method of Correcting ROM Bit Errors in a ROM Embedded DRAM By Programming a ROM Section Of a ROM Embedded DRAM, Encoding on the ROM Embedded DRAM in Error Correcting Code (ECC) Circuitry the ROM Data and Decoding Read ROM Data Before Presenting the Data to a User, classified in class 714, subclass 763.

The inventions are distinct, each from the other because of the following reasons: Inventions Group I, ROM Embedded DRAM wherein ROM Cells are Formed by Programming DRAM Cells within a DRAM Array and Correction Circuitry is Fabricated on and Integrated with the DRAM, and Group III, A Method of Operating a ROM Embedded DRAM by Receiving a Row and Column Address to Read Data from a ROM Section and Reading an Encoded ROM Bit, are related as product and process of use. The inventions can be shown to be distinct if either or both of the following can be shown: (1) the process for using the product as claimed can be practiced with another materially different product or (2) the product as claimed can be used in a materially different process of using that product (MPEP § 806.05(h)). In the instant case the

process can be practiced on ROM Embedded DRAM with error correction circuitry separate from the ROM Embedded DRAM and the product, ROM Embedded DRAM, can be used for row or column redundancy replacement.

Inventions Group II, Method of Fabricating a ROM Embedded DRAM by Forming an Array of DRAM Cells having a First Portion of ROM Cells and a Second Portion of DRAM Cells and Programming a ROM Portion of the DRAM Cells as ROM Bits, and Group III, A Method of Operating a ROM Embedded DRAM by Receiving a Row and Column Address to Read Data from a ROM Section and Reading an Encoded ROM Bit, are related as mutually exclusive species in an intermediate-final product relationship. Distinctness is proven for claims in this relationship if the intermediate product is useful to make other than the final product (MPEP § 806.04(b), 3rd paragraph), and the species are patentably distinct (MPEP § 806.04(h)). In the instant case, the intermediate product, Group II, Method of Fabricating a ROM Embedded DRAM by Forming an Array of DRAM Cells having a First Portion of ROM Cells and a Second Portion of DRAM Cells and Programming a ROM Portion of the DRAM Cells as ROM Bits, is deemed to be useful as ROM Embedded DRAM used for row or column redundancy replacement and the inventions are deemed patentably distinct since there is nothing on this record to show them to be obvious variants. Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the

examiner finds one of the inventions anticipated by the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Inventions Group III, A Method of Operating a ROM Embedded DRAM by Receiving a Row and Column Address to Read Data from a ROM Section and Reading an Encoded ROM Bit, and Group IV, ROM Embedded DRAM with an Error Correction Element Containing Encoded ROM Bit Data or each ROM Bit, are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the process can be practiced on ROM Embedded DRAM with error correction circuitry separate from the ROM Embedded DRAM and the product, ROM Embedded DRAM, can be used for row or column redundancy replacement.

Inventions Group III, A Method of Operating a ROM Embedded DRAM by Receiving a Row and Column Address to Read Data from a ROM Section and Reading an Encoded ROM Bit, and Group V, A Method of Repairing ROM Bit Errors in a ROM Embedded DRAM by Encoding ROM Data in Error Correction Circuitry, Determining Whether the ROM Bit Data is Correct and Correcting the ROM Bit Data if the ROM Bit Data and the Stored Data Are Different, are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are

shown to be separately usable. In the instant case, invention Group III, A Method of Operating a ROM Embedded DRAM by Receiving a Row and Column Address to Read Data from a ROM Section and Reading an Encoded ROM Bit, has separate utility such as in ROM Embedded DRAM that is factory programmed. See MPEP § 806.05(d).

Inventions Group III, A Method of Operating a ROM Embedded DRAM by Receiving a Row and Column Address to Read Data from a ROM Section and Reading an Encoded ROM Bit, and Group VI, A Method of Correcting ROM Bit Errors in a ROM Embedded DRAM By Programming a ROM Section Of a ROM Embedded DRAM, Encoding on the ROM Embedded DRAM in Error Correcting Code (ECC) Circuitry the ROM Data and Decoding Read ROM Data Before Presenting the Data to a User, are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group III, A Method of Operating a ROM Embedded DRAM by Receiving a Row and Column Address to Read Data from a ROM Section and Reading an Encoded ROM Bit, has separate utility such as in ROM Embedded DRAM that is factory programmed. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group III is not required for Group I and vice a versa, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group III is not required for Group II and vice a versa, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group III is not required for Group III and vice a versa, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group III is not required for Group IV and vice a versa, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group III is not required for Group V and vice a versa, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group III is not required for Group VI and vice a versa, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Daniel Polglaze on 08 April 2004 a provisional election was made without traverse to prosecute the invention of Group III, claims 9-14 and 24-26. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-8 and 15-23 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: '100'. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 11 and 12 are objected to because of the following informalities: claim 11 is incorrectly numbered and should depend from claim 10 as per the Examiner's conversation with the Attorney of Record (see Interview Summary). Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 9-14 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over McConnell; Roderick et al. (US 5986952 A, hereafter referred to as McConnell).

35 U.S.C. 103(a) rejection of claims 9 and 24.

McConnell teaches a method of operating a ROM embedded DRAM (col. 2, lines 40-67 and col. 1, lines 60-67 in McConnell teach that a DROM is a memory device with a ROM section built out of DRAM cells and embedded in DRAM so that some of the DRAM cells still function as DRAM, hence DROM is ROM embedded DRAM; Note: in Figure 1 of McConnell memory cells 11 and 13 are ROM cells and memory cells 12 are DRAM cells), comprising: receiving a row and column address to read data from a ROM section (Figure 1 of McConnell teaches the use of bit line addresses BADR and word line addresses WADR for accessing memory during read/write operations; Note: a bit line address BADR is a row address and a word line address WADR is a column

address; Note also that claim 3 in McConnell teaches that memory is addressable and accessible for reading out data in units and that col.1, lines 16-28 in McConnell teach that units can be word or bit lines; Note: if the units are bit lines, then both the bit line row address BADR and the word line column address WADR are required to access data during read out since data is read out of bit lines, hence McConnell teaches receiving a bit line row addresses BADR and word line column addresses WADR to read data from a ROM unit); reading an encoded ROM bit using an error correcting code decoder (col. 4, lines 32-40 in McConnell teach that the E3 units are used to store parity data for the E1 units, hence the ROM units are encoded; col. 4, lines 62-67 in McConnell teach that error correction is carried out by repair device 5 using error correction codes, hence repair device 5 is an error correcting circuitry for decoding the read ROM bit; Note: error correcting circuitry repair device 5 is used to read); and correcting the read ROM bit if necessary (col. 4, lines 62-67 in McConnell teach the use of error correction codes for performing error correction).

However McConnell does not explicitly teach the specific use of presenting the corrected ROM bit as output data.

The Examiner asserts that memory is useless unless connected to other electronic devices needing storage. It is also obvious that corrected data would be provided to an application hardware device since correct data is necessary for correct system operation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of McConnell by including use of

presenting the corrected ROM bit as output data. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of presenting the corrected ROM bit as output data would have provided the opportunity to maintain correct system operation.

35 U.S.C. 103(a) rejection of claim 10.

McConnell teaches decoding the read ROM bit with error correcting circuitry (col. 4, lines 62-67 in McConnell teach that error correction is carried out by repair device 5 using error correction codes, hence repair device 5 is an error correcting circuitry for decoding the read ROM bit); comparing the decoded ROM bit with the actual ROM bit (Note: error correction is a means for comparing decoded bits with actual ROM bits by comparing the read parity from the E3 units with the newly generated parity during decoding); and correcting if the decoded ROM bit differs from the read ROM bit (col. 4, lines 62-67 in McConnell teach that the error correction codes are used for performing error correction).

35 U.S.C. 103(a) rejection of claim 11.

Col. 4, lines 62-67 in McConnell teach that error correction is carried out by repair device 5 using error correction codes, hence repair device 5 is an error correcting circuitry for error correcting.

35 U.S.C. 103(a) rejection of claim 12.

McConnell teaches generating an ECC corrected ROM bit from a read ROM bit (col. 4, lines 62-67 in McConnell teach that error correction is carried out by repair device 5 using error correction codes); comparing the ECC corrected bit with the read ROM bit (col. 3, lines 22-25 in McConnell teach that read out data is compared with actual written data; Note: error correction is used in the read process, hence read data is error corrected data); and correcting the read ROM bit if the ECC corrected ROM bit and the read ROM bit do not match (col. 3, lines 22-28 in McConnell teach that the ROM bit is corrected by matching the address to a replacement E2 unit).

35 U.S.C. 103(a) rejection of claim 13.

McConnell teaches error correcting with parity checking (col. 3, lines 10-13 in McConnell).

35 U.S.C. 103(a) rejection of claim 14.

McConnell teaches comparing the parity check bit with the read ROM bit (Note: error correction is a means for comparing decoded bits with actual ROM bits by comparing the read parity ROM bits from the E3 units with the newly generated parity during decoding); and inverting the read ROM bit if the parity bit indicates an error (col. 4, lines 62-67 in McConnell teach that the error correction codes are used for performing error correction).

35 U.S.C. 103(a) rejection of claim 25.

McConnell substantially teaches the claimed invention described in claim 24 (as rejected above). In addition, McConnell teaches reading a unit of ROM data (Note that claim 3 in McConnell teaches that memory is addressable and accessible for reading out data in units and that col.1, lines 16-28 in McConnell teach that units can be word or bit lines); decoding the unit of ROM data (col. 4, lines 62-67 in McConnell teach that error correction is carried out by repair device 5 using error correction codes, hence repair device 5 is an error correcting circuitry for decoding the read ROM unit); and determining if the ROM data is correct (Note: error correction is a means for comparing decoded bits with actual ROM bits by comparing the read parity from the E3 units with the newly generated parity during decoding to determine of the data is correct). However McConnell does not explicitly teach the specific use of a byte size unit.

The Examiner asserts that col.1, lines 16-28 in McConnell teach that units can be word or bit lines as an example but explicitly leaves the size of a unit open so that embodiment using any other unit size is an obvious engineering design choice. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to with the teachings of McConnell by including use of a byte size unit. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a byte size unit would have provided the opportunity to implement a particular embodiment of the McConnell based on obvious engineering design choices such as memory width bus width, error correction code, etc.

35 U.S.C. 103(a) rejection of claim 26.

McConnell teaches error correcting with parity checking (col. 3, lines 10-13 in McConnell).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Asami; Kazuo (US 5467357 A) teaches an EEPROM apparatus built, for example, in a one-chip microcomputer used for an IC card.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Art Unit 2133